REMARKS

Claims 7, 8, 16, 17, 24 and 25 stand rejected under 35 U. S. C. 112, 1st paragraph, as failing to comply with the enablement requirement. The applicant has amended claims 7, 8, 16, 17, 24 and 25.

Claims 7, 8, 16, 17, 24 and 25 stand rejected under 35 U. S. C. 112, 2nd paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The applicant has amended claims 7, 8, 16, 17, 24 and 25.

The Examiner has objected to the disclosure and has asserted that the specification fails to provide a detailed description of a HyperTransport™. The Applicant respectfully submits that the specification provides adequate description. Specifically, the applicant discloses at page 7, line 5 through page 8, line 23

> "Computer system 10 includes process nodes 12A-12D each interconnected by coherent packet interfaces 15A-D. Each link of coherent packet interface 15 may form a high-speed point-to-point link. Process nodes 12A and 12B are also coupled to system memory 17A and 17B, respectively. Process nodes 12A-D may each include one or more processors, a memory controller for managing memory transactions to memory such as memories 17A-B. Computer system 10 also includes an I/O node 20 and an I/O node 30. I/O node 20 is coupled to process node 12A via a non-coherent packet interface 50A. I/O node 20 is connected to I/O node 30 in a chain topology by non-coherent packet interface 50B. Process node 12A is illustrated as a host node and may include a host bridge for communicating with I/O node 20 via non-coherent packet interface 50A. Process nodes 12B-D may also include host bridges for communication with other I/O nodes (not shown). The non-coherent packet interface links formed by non-coherent packet interface 50A-B may also be referred to as a point-to-point links. ...
>
> In the illustrated embodiment, each link of coherent packet interface 15 is implemented as sets of unidirectional lines (e.g. lines 15A are used to transmit packets from processing node 12A to processing node 12B and lines 15B are used to transmit packets from processing node 12B to processing node 12C). Other sets of lines 15C-D are used to transmit packets between other processing nodes as illustrated in FIG. 1. The

coherent packet interface 15 may be operated in a cache coherent fashion for communication between processing nodes ("the coherent link"). Further, non-coherent packet interface 50 may be operated in a non-coherent fashion for communication between I/O nodes and between I/O nodes and a host bridge such as the host bridge of process node 12A ("the non-coherent link"). The non-coherent links may also be implemented as sets of unidirectional lines (e.g. lines 50A are used to transmit packets from processing node 12A to I/O node 20 and lines 50B are used to transmit packets from I/O node 20 to I/O node 30). The interconnection of two or more nodes via coherent links may be referred to as a "coherent fabric". Similarly, the interconnection of two or more nodes via non-coherent links may be referred to as a "non-coherent fabric". It is noted that a packet to be transmitted from one processing node to another may pass through one or more intermediate nodes. For example, a packet transmitted by processing node 12A to processing node 12C may pass through either processing node 12B or processing node 12D as shown in FIG. 1. Similarly, packets transmitted to I/O node 30 may first pass through I/O node 20. Any suitable routing algorithm may be used. As denoted by the dashed line surrounding process nodes 12B-D, other embodiments of computer system 10 may include more or fewer processing nodes than the embodiment shown in FIG. 1.

Process nodes 12A-12D may include one or more processors (not shown). NC packet interfaces 50A-50B may be compatible with non-coherent HyperTransport™ technology."

In addition, the Applicant discloses, in greater detail, specific aspects of the interface (of which, HyperTransport™ is merely one example) at page 9, line 1 through page 11, line 10.

Claims 1-6, 9-15, 18-23, and 26 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ajanovic et al. (U.S. Patent Number 6,516,375) (hereinafter 'Ajanovic'). The Applicant respectfully traverses these rejections.

Claims 7, 8, 16, 17, 24 and 25 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ajanovic in view of Hayter et al. (U. S. Patent Number 6,574,708) (hereinafter 'Hayter'). The Applicant respectfully traverses these rejections.

The applicant discloses at page 13, lines 4-25

"I/O node 100 includes a transceiver unit 110 which is coupled to a link of NC packet interface 50B and to an internal packet bus interface 130 via an internal packet interface link 115. I/O node 100 also includes an I/O hub 120 which is also coupled to internal packet bus interface 130 via an internal packet interface link 125. I/O hub 120 is coupled to peripheral bus 36 and to LPC bus 37. I/O node 100 further includes a graphics bus interface 150 which is coupled to a graphics engine 160 through graphics bus 35. Graphics bus interface 150 is coupled to receive transactions from transceiver unit 110 through internal packet bus interface 130 and internal packet interface link 155. Graphics engine 160 may be connected to a display such as display 38 of FIG. 1.

Transceiver 110 may be configured to transmit and receive packets over NC packet interface link 50B. Transceiver 110 may include buffers and control logic (not shown) necessary to buffer incoming packets. Transceiver 110 may also include interface logic (not shown) for transmitting and receiving packets within I/O node 100 via internal packet interface link 115.

I/O hub 120 may include circuitry (not shown in FIG. 2) which may be translate packets into an I/O protocol suitable for use by I/O hub 120. Additionally, I/O hub 120 may include circuitry (also not shown in FIG. 2) which may translate transactions from an I/O protocol suitable for use by I/O hub 120 into packets for transmission on internal packet link 125. Further, I/O hub 120 may include circuitry which provides peripheral bus support for peripheral bus 26 and for LPC bus 37."

Accordingly, Applicant's claim 1 recites

"an input/output node for a computer system, said input/output node comprising:

a transceiver unit implemented on an integrated circuit chip, wherein said transceiver unit is configured to receive and transmit packets on a point-to-point link of a packet interface;

a graphics engine implemented on said integrated circuit chip, wherein said graphics engine is coupled to receive graphics packets received by said transceiver unit and is configured to render digital image information in response to receiving said graphics packets; and

an I/O hub implemented on said integrated circuit chip, wherein said I/O hub is coupled to receive I/O packets corresponding to packets received by said transceiver unit and is configured to initiate bus cycles corresponding to said I/O packets upon a peripheral bus." (Emphasis added)

The Examiner appears to assert Ajanovic teaches an I/O node for computer system comprising "a transceiver unit implemented on integrated circuit chip when the transceiver unit is configured to receive and transmit packets on a point-to-point link of a packet interface [see column 3, lines 35-67; column 4, lines 1-44; figure 1, elements 140, 142, 143]." In addition, the Examiner asserts Ajanovic teaches "a graphics engine implemented on the integrated circuit chip when the graphics engine is coupled to receive graphics packets received by the transceiver unit and is configured to render digital information in response to receiving the graphics packets [see column 2, lines 50-67; column 3, lines 1-33; and figure 1 - elements 120, 124 and 125]."

The Applicant is unclear about the Examiners later assertion "although Ajanovic teaches interfacing means to connect various peripherals to allow exchange of information [see column 4, lines 16-44], a Ajanovic is silent about using a transceiver to receive and transmit information to and from the peripherals."

The Applicant respectfully disagrees with the Examiner's assertions. Specifically, a Ajanovic teaches at column 3, lines 4-8 "graphics interface controller 124 is coupled to the graphics accelerator 125 through a suitable interface, such as an accelerated graphics Port (AGP) or a hub interface for example." The Applicant notes graphics interface controller 124 of Ajanovic is not a graphics engine as recited in the Applicant's claim 1. The applicant further notes that the graphics accelerator 125 of Ajanovic is not implemented on the MCH 120 and as noted above graphics accelerator 125 is coupled to graphics interface controller 124 through an AGP interface.

Accordingly, Ajanovic does not to teach or disclose "a graphics engine implemented on said integrated circuit chip, wherein said graphics engine is coupled to receive graphics packets received by said transceiver unit" as recited in Applicant's claim 1. In addition, Ajanovic does not teach or disclose a graphics engine and an I/O node both implemented on the same integrated circuit chip wherein the I/O node is "coupled to receive I/O packets corresponding to packets received by said transceiver unit..." as recited in Applicant's claim 1.

Furthermore, applicant's claim 3 recites "a graphics bus interface implemented on said integrated circuit chip, wherein said graphics bus interface is coupled to receive and to translate said graphics packets into graphics commands suitable for transmission upon a graphics bus." The applicant respectfully submits that the I/O node includes both a graphics bus interface and a graphics engine. However the applicant's graphics bus interface may be coupled to an external graphics engine similar to graphics interface 124 and graphics accelerator 125 of Ajanovic. Thus it is clear that the Applicant's graphics engine, as recited in claim 1, is not taught or suggested by Ajanovic.

The applicant respectfully submits that claim 1, along with its dependent claims, patentably distinguishes over Ajanovic and over Ajanovic in view of Hayter for the reasons given above.

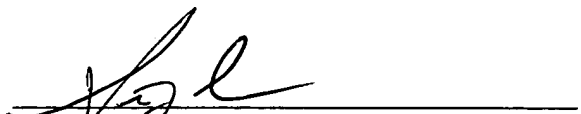
Likewise, claims 10 and 19 recited features similar to claim 1. Thus, claims 10 and 19, along with their respective dependent claims, are believed to patentably distinguish over Ajanovic and over Ajanovic in view of Hayter for at least the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-73600/BNK.

Respectfully submitted,



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